CLAIMS:

1. A method for fabricating a semiconducting layer with reduced soft error rates comprising:

providing a semiconductor substrate;

forming a first semiconductor layer over the substrate, said first semiconductor layer being comprised of a first semiconductor material and having a vertical extent defined by an upper extent of the first semiconductor material and a lower extent of the first semiconductor material;

forming a generally constant electric field across the vertical extent of the first semiconductor material, wherein a charge which occurs within the first semiconductor layer is influenced toward the semiconductor substrate; and

forming a device layer in which a semiconductor device may be fabricated.

2. The method for fabricating recited in claim 1 above, wherein forming a first semiconductor layer over the substrate further comprises:

establishing a first dopant concentration;

establishing a second dopant concentration; and

depositing the first semiconductor material in a graded dopant concentration profile, said graded dopant concentration having said first dopant concentration at the lower extent of the semiconductor material, said second dopant concentration at the upper extent of the semiconductor material, and dopant concentrations between said first dopant concentration and said second dopant concentration between the upper extent and lower extent of the first semiconductor material.

3. The method for fabricating recited in claim 2 above, wherein establishing said second dopant concentration is based on said semiconductor device to be fabricated in the device layer.

4. The method for fabricating recited in claim 2 above, wherein said device layer is formed within the vertical extent of first semiconductor material.

5. The method for fabricating recited in claim 3 above further comprises:

forming a second electric field at the lower extent of the first semiconductor material.

6. The method for fabricating recited in claim 5 above, wherein forming said second electric field further comprises:

determining a dopant concentration of said semiconductor substrate;

selecting the second dopant concentration based on said dopant concentration of said semiconductor substrate, wherein said second dopant concentration is different from said dopant concentration of said semiconductor substrate.

7. The method for fabricating recited in claim 3 above further comprises:

forming a second electric field below the first semiconductor material.

8. The method for fabricating recited in claim 7 above, wherein said semiconductor substrate is a P+ semiconductor substrate, and forming said second electric field further comprises:

forming an undoped intrinsic layer over said P+ semiconductor substrate; and

forming said first semiconductor layer over the undoped intrinsic layer.

9. The method for fabricating recited in claim 7 above, wherein said semiconductor substrate is a P- semiconductor substrate, and forming said second electric field further comprises:

forming a buried n-layer over said P- semiconductor substrate;

forming an undoped intrinsic layer over said buried n-layer; and

forming said first semiconductor layer over the undoped intrinsic layer.

10. The method for fabricating recited in claim 1 above, wherein forming the first semiconductor layer further comprises epitaxially forming the first semiconductor layer.

11. A semiconducting structure having reduced with soft error rates comprising:

a semiconductor substrate;

a first semiconductor layer over the substrate, said first semiconductor layer being comprised of a first semiconductor material and having a vertical extent defined by an upper extent of the first semiconductor material and a lower extent of the first semiconductor material;

a generally constant electric field across the vertical extent of the first semiconductor material, wherein a charge which occurs within the first semiconductor layer is influenced toward the semiconductor substrate; and

a device layer in which a semiconductor device may be fabricated.

12. The semiconducting structure recited in claim 11 above, wherein the first semiconductor layer over the substrate further comprises a graded dopant concentration, said graded dopant concentration having a first dopant concentration established at the lower extent of the semiconductor material, a second dopant concentration established at the upper extent of the semiconductor material and a plurality of dopant concentrations

between said first dopant concentration and said second dopant concentration between the upper extent and lower extent of the first semiconductor material.

13. The semiconducting structure recited in claim 12 above, wherein said second dopant concentration is based on said semiconductor device to be fabricated in the device layer.

14. The semiconducting structure recited in claim 12 above, wherein said device layer is formed within the vertical extent of first semiconductor material.

15. The semiconducting structure recited in claim 13 above further comprises:

a second electric field formed at the lower extent of the first semiconductor material.

16. The semiconducting structure recited in claim 15 above, wherein the second dopant concentration is based on a dopant concentration of said semiconductor substrate, wherein said second dopant concentration is different from said dopant concentration of said semiconductor.

17. The semiconducting structure recited in claim 13 above further comprises:

a second electric field below the first semiconductor material.

18. The semiconducting structure recited in claim 17 above, wherein said semiconductor substrate is a P+ semiconductor substrate, and said semiconducting structure further comprises:

an undoped intrinsic layer formed over said P+ semiconductor substrate and under said first semiconductor layer.

19. The semiconducting structure recited in claim 17 above, wherein said semiconductor substrate is a P- semiconductor substrate, and semiconducting further comprises:

a buried n-layer formed over said P- semiconductor substrate; and

an undoped intrinsic layer formed over said buried n-layer and formed under said first semiconductor layer.

20. A method for fabricating recited in claim 11 above, wherein the first semiconductor layer is an epitaxial first semiconductor layer.